REMARKS

Summary of Office Action

Claims 1-25 were pending in this application.

Claims 1-25 were been rejected under 35 U.S.C. § 103(a) as being obvious from Peng U.S. Patent No. 5,594,675 ("Peng") in view of Graybill U.S. Patent No. 5,179,714 ("Graybill"). Claim 15 was rejected under 35 U.S.C. § 103(a) as being obvious from Washakowski et al. U.S. Patent Application Publication No. 2005/0238117 ("Washakowski") in view of Graybill. Claims 16-25 were rejected under 35 U.S.C. § 103(a) as being obvious from Washakowski and Graybill further in view of Peng.

Summary of Applicant's Reply

Applicant has amended claims 1, 2, 6, 15, 16, 21 and 22 and has added new claims 26 and 27 in order to more particularly define the claimed invention. No new matter has been added. The amendments and new claims are fully supported by the originally-filed application.

Applicant respectfully traverses the Examiner's rejections.

Applicant's Reply

Claims 1-21

The Examiner rejected claims 1-25 under 35 U.S.C. § 103(a) as being obvious from Peng in view of Graybill. Applicant respectfully traverses this rejection.

Applicant's invention, as defined by amended independent claims 1 and 15, is directed to DSP circuitry that independently processes a plurality of multi-channel data signals. The circuitry includes, *inter alia*, first and second columns of registers and interconnection circuitry that allows a first of the channels to be selectively shifted through (or registered in), at the same time, the registers in the first and second columns. The interconnection circuitry also allows the output of the first column to be selectively shifted through (or registered in) the registers in the second column instead of the first channel that is received by the first and second columns at the same time.

Peng generally discusses a digital FIR filter. FIG. 11 shows multiple selector circuits 735 each including a shift register 734-u for storing tap coefficient values and a multiplexer 732-u connected to each shift register. The multiplexer can select either the coefficient value output from its own shift register or the value output from a previous selector circuit 735 via line 736. (Peng, FIG. 11 and col. 17, lines 5-24.)

Graybill generally discusses a parallel bit serial data processor. FIG. 12 shows registers 120 arranged in columns *i* and multiplexers 330 connected to each of the registers. Multiplexers 330 provide to each register 120 in the columns *i* either a global input *NCMGCi* unique to column *i* or the output of a previous register in the column *i*. (Graybill, Abstract; FIG. 12; and col. 9, lines 5-25.)

The Examiner acknowledges that Peng does not show or suggest bypassing any register or registers that precede said register in said respective column but contends that such implementation is similar to a shift register which is an obvious matter of design choice and additionally cites Graybill as allegedly making up for this deficiency (Office Action, pages 3 and 4). Applicant respectfully traverses this rejection.

First, applicant respectfully submits that it is not an obvious matter of design choice and Graybill does not show or suggest interconnection circuitry that allows a first channel to be selectively shifted through (or registered in), at the same time, the registers in first and second columns of registers, as defined by applicant's claims 1 and 15. Instead, in Graybill each of the alleged columns of registers 120 receives a different global input *NCMGC* unique to the column and thus Graybill does not show or suggest a channel being registered in first and second columns at the same time, as required by applicant's claims. Moreover, although shift registers allegedly have a similar implementation as the Graybill shift registers, it is not an obvious matter of design choice to register a channel in first and second columns at the same time. Thus, contrary to the Examiner's assertions, Graybill does not make up for the deficiencies of Peng relative to the rejection and it would not be an obvious matter of design choice to arrive at applicant's invention.

Second, applicant respectfully submits that Peng and Graybill, whether taken alone or in combination, do not show or

suggest allowing an output of a first column to be selectively shifted through registers in a second column instead of a first channel that is received by the first and second columns at the same time, as defined by applicant's claims 1 and 15. Instead, in Peng each column shifts either the column's own output or the output of a previous column and thus Peng does not show or suggest a channel that is received by two columns at the same time. In particular, because Peng discusses each subsequent column receiving a delayed version of the input 736, Peng does not show or suggest two columns receiving a channel at the same time. Moreover, the multiplexers preceding each column in Peng select between an output from a previous column and an output from their own column and thus do not allow an output from a first column to be shifted through a second column (i.e., a different column) instead of a first channel that is received at the same time by both columns (i.e., the particular column output in Peng that can be shifted into another column is not a first channel received by two columns at the same time). Additionally, as discussed above, Graybill also does not show or suggest a channel being received and registered in first and second columns at the same time. Therefore, Peng and Graybill, whether taken alone, or in combination, do not show or suggest all the features of applicant's claims.

Accordingly, applicant respectfully submits that independent claims 1 and 15 and claims 2-14 and 16-25 that depend, directly or indirectly, from claim 1 or 15, are allowable over the prior art of record.

Claims 15-21

The Examiner rejected claim 15 under 35 U.S.C. § 103(a) as being obvious from Washakowski in view of Graybill. The Examiner rejected claims 16-25 under 35 U.S.C. § 103(a) as being obvious from Washakowski and Graybill further in view of Peng. Applicant respectfully traverses these rejections.

The Examiner acknowledges that Washakowski does not show or suggest bypassing any register or registers that precede said register in said tap delay line circuitry but contends that such implementation is similar to a shift register which is an obvious matter of design choice and nevertheless cites Graybill as allegedly making up for this deficiency (Office Action, pages 11 and 12). Applicant respectfully traverses this rejection.

For the reasons stated above with respect to Peng, applicant respectfully submits that Washakowski and the suggested modification using shift registers as an obvious matter of design choice does not show or suggest all the features of applicant's claimed invention. Additionally, as stated above, Graybill does not show or suggest interconnection circuitry that allows a first of multiple channels to be selectively shifted through (or registered in), at the same time, the registers in first and second columns and therefore does not make up for the deficiencies of Washakowski in that regard.

Furthermore, applicant respectfully submits that Washakowski does not show or suggest interconnection circuitry that allows a first of multiple channels to be selectively

shifted through (or registered in), at the same time, the registers in first and second columns, as defined by applicant's claims 1 and 15. Instead, Washakowski discusses registering two different channel components *I* and *Q* in two columns 440I and 440Q and thus does not show or suggest registering the same data from a channel in two columns at the same time. Therefore, Washakowski does not make up for the deficiencies of Peng and Graybill relative to the rejections of claims 1 and 15.

Peng, cited as allegedly showing features of applicant's dependent claims, does not make up for the deficiencies of Washakowski or Graybill relative to the rejection.

Accordingly, applicant respectfully submits that independent claim 15 and claims 16-21 that depend, directly or indirectly, therefrom, are allowable over the prior art of record.

New Claims

Applicant has added new claims 26 and 27 in order to more particularly define the claimed invention. New claims 26 and 27 depend respectively from patentable claim 1 and 15 and therefore also are patentable.

Conclusion

The foregoing demonstrates that claims 1-27 are allowable. This application is therefore in condition for allowance. Reconsideration and prompt allowance are accordingly respectfully requested.

Respectfully submitted,

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